What is claimed is:

1. A transmitter, wherein the transmitter is a Very High Speed Digital Subscriber Line (VDSL) transmitter comprising:

- a first input for receiving data (DATA);

- a second input for receiving a network timing reference signal (CLK2);

- a third input for receiving a transmitter sampling clock signal (CLK1);

- an output for providing data frames (FRAME);

- embedding circuitry (EMBED) coupled between said first input and said output, wherein the embedding circuitry is adapted to embed said data in said data frames (FRAME) and to output said data frames to said output; and

- phase measurement circuitry (PHASE) coupled to said second input and responsive to a local timing reference signal (R), said local timing reference signal (R) being derived from said transmitter sampling clock signal (CLK1), wherein said phase measurement circuitry (PHASE) is adapted to measure a phase offset value (P) between said network timing reference signal (CLK2) and said local timing reference signal (R), and to output said phase offset value (P) to said embedding circuitry (EMBED);

wherein said embedding circuitry (EMBED) is further configured so as to embed in one of said data frames (FRAME) a change of said phase offset value (P) from a previously measured phase offset value (P).

2. A Very High Speed Digital Subscriber Line (VDSL) transmitter according to claim 1, wherein said local timing reference signal (R) is derived from said transmitter sampling clock signal (CLK1) by dividing said transmitter sampling clock signal (CLK1)

through an appropriate number.

3. A Very High Speed Digital Subscriber Line (VDSL) transmitter according to claim 1, wherein a change of said phase offset value (P) is embedded in each VDSL data frame (FRAME).

4. A Very High Speed Digital Subscriber Line (VDSL) transmitter according to claim 1, wherein said data frame (FRAME) includes fast bytes at least some of which are used for transporting operational channel related information, and wherein said change of said phase offset value (P) is embedded in said fast bytes.

5. A Very High Speed Digital Subscriber Line (VDSL) transmitter according to claim 1, wherein said change of said phase offset value (P) is expressed as a 2's complement number of clock cycles of said transmitter sampling clock signal (CLK1).

6. A receiver, wherein the receiver is a Very High Speed Digital Subscriber Line (VDSL) comprising:

- a receiver input for receiving data frames (FRAME);

- a clock input for receiving a receiver sampling clock signal (CLK1');

- a first receiver output for providing a received output signal (DATA') and a second receiver output for providing a clock output (CLK2');

- retrieving circuitry (D-EMBED) adapted to retrieve incoming data (DATA') from said data frames (FRAME), to output said retrieved data (DATA') to said first receiver output, and to retrieve a change of a phase offset value (P) from a previously recovered phase offset value (P) out of a reserved field within said data frames (FRAME);

- local timing reference signal circuitry adapted to generate a local timing reference signal (R') from said receiver sampling clock signal (CLK1'); and

- a clock generator (GEN) having a first input for receiving said change of said phase offset value (P), and a second input for receiving said local timing reference signal (R'), wherein said clock generator (GEN) is configured so as to generate a clock signal (CLK2') having a phase offset from said local timing reference signal (R') generally equal to said phase offset value (P).

7. A Very High Speed Digital Subscriber Line (VDSL) receiver according to claim 6, wherein said local timing reference signal (R') is derived from said receiver sampling clock signal (CLK1') by dividing said receiver sampling clock signal (CLK1') through an appropriate number.

8. A Very High Speed Digital Subscriber Line (VDSL) receiver according to claim 6, wherein a change of said phase offset value (P) is embedded in each VDSL data frame (FRAME).

9. A Very High Speed Digital Subscriber Line (VDSL) receiver according to claim 6, wherein said data frame (FRAME) includes fast overhead bytes at least some of which are used for transporting operational channel related information, and wherein said change of said phase offset value (P) is retrieved from said fast overhead bytes.

10. A Very High Speed Digital Subscriber Line (VDSL) receiver according to claim 6, wherein said change of said phase offset value (P) is expressed as a 2's complement number of clock cycles of said receiver sampling clock signal (CLK1').